Georgios Passas

ASIC DEVELOPER & RESEARCHER

PROFILE

Proven technical ownership and capacity to develop ASICs at all architecture, design, verification, and implementation levels. Forward thinking and strong problem solver with attention to detail.

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georgiospassas.com

Asperudlia 73, 1258, Oslo

Greek, Male, Born 1981

EDUCATION

PhD Computer Science **2004-2012**
Univ. of Crete, Greece

Thesis: VLSI Microarch's for High Radix Crossbars
Maria M. Manassaki Scholarship of Excellence, 2011

BSc Computer Science **1999-2004**
Univ. of Crete, Greece

Panhellenic exams: Accepted in 3rd place in deprtmnt

5ο Λύκειο Θεσσαλονίκης **1996-1999**
Thessaloniki, Greece

TRAININGS

MHFA England Mental Health First Aid, 2021

Cadence Genus, Innovus, Tempus, 2020

Sunburst Design SV & UVM, 2018

ISTQB Cert. Tester, Foundation Level, 2018

INDUSTRIAL WORK EXPERIENCE

Hardware Engineer and Chairman **2022/03 - now**
GP Consulting AS

- Developed ISO 26262 extensions for auto-generated register files.
- Ongoing service available upon request

Senior Hardware Engineer **2019/09 - 2022/03**
Arm Norway, Trondheim

Design, verification, and implementation of Mali GPU components.

Senior Hardware Engineer **2018/09 - 2019/09**
Numascale & Simula, Oslo, Norway

UVM verification of directory memory and protocol FSM units in a node controller ASIC for cache-coherent scale-up systems.

Digital Design Engineer **2017/10 - 2018/09**
Swarm64, Berlin, Germany

Updates and development of database FPGA accelerator testbenches using UVM and adhoc (svunit) methodologies. Followed agile principles.

International Student Intern **2007/10 - 2008/02**
Sun Labs, Menlo Park, CA, USA

Updates to in-house event-driven queueing system simulator (C/C++) for Proximity Communication switches.

MILITARY SERVICE

Programmer-Analyst **2012/06 - 2013/02**
Ministry of National Defence, Athens, Greece

Served as administrator-developer of soldier-entry database front-end within program "ESEP": Unified System for Personnel Management

ACADEMIC WORK EXPERIENCE

Postdoc Researcher **2013/02 - 2015/09**
Barcelona Supercomputing Center, Spain

Developed model in gem5 full CMP simulator (C/C++/Python) for crossbar and mesh NoC, ran PARSEC and SPLASH multi-threaded benchmarks, and plotted a performance comparison as contribution to a EU project. https://arxiv.org/abs/1607.07766

SKILLS

Hardware SV — UVM, IMC — Formal with Jasper Gold — Veripool Autos — Linting — DVE, Simvision — Cadence Genus-Innovus-Tempus — LEC — FPGA — IPXACT, SystemRDL, UVM RAL

Software C/C++ — Bash, Python

Devops Jenkins — TeamCity — ES Kibana, Grafana

Collaboration Tools Jira — Confluence — Git, SVN, ClearCase — Gerrit, BitBucket, Gitlab — Scrum

Simulation Gem5 — Queueing System Simulation

Office TEX — MS —MacOS

ACADEMIC WORK EXPERIENCE

Research Employee **2012/02 - 2012/06**

FORTH-ICS, Crete, Greece

As co-instructor developed lectures and project for new Univ. Crete graduate course “CS-590.22”: CMOS Technology for Computer Architects.

PhD Student **2004/02 - 2012/02**

FORTH-ICS, Crete, Greece

Designed, synthesized, laid out, and optimized 128×128 32-bit crossbar switch @ 750MHz in 14mm2 in 90nm CMOS, including priority circuits for arbiters. Custom and hierarchically placed gates to achieve virtually 100% layout utilization using over gates and memory wire routing. During postdoc ported circuit to 45nm (1GHz, 6mm2) and published to IEEE Micro. Wrote ad-hoc event-driven queueing-system simulators (C/C++) for variable-packet-size crossbar switches. Published to conferences ICC and HPSR.

ACADEMIC RECORD

Patents

G. Passas, H. Eberle, N. Gura, W. Olesinski: “Fast and Fair Arbitration on a Data Link”, U.S. Patent, USPTO#7965705, 2011.

A. Vijayashekar, J. Pennala, G. Passas: “Data Processing Systems”, U.S. Patent, USPTO#11489940, 2022.

Journal Articles

G. Passas, M. Katevenis, D. Pnevmatikatos: “The Combined Input-Output Queued (CIOQ) Crossbar Architecture for High-Radix On-Chip Switches”, IEEE Micro gen’l issue, 5000 words, 2015.

G. Passas, M. Katevenis, D. Pnevmatikatos: “Crossbar NoC’s Are Scalable Beyond 100 Nodes”, IEEE Tran. Computer-Aided Design Integrated Circuits and Systems (TCAD), 2012, 13 pg

Conference Proceedings

G. Passas, M. Katevenis, D. Pnevmatikatos: “VLSI Micro-Architectures for High-Radix Crossbar Schedulers”, ACM/IEEE Symp. Networks-on-Chip (NOCS 2011), Pittsburgh, 2011, 8 pg.

G. Passas, M. Katevenis, D. Pnevmatikatos: “A 128x128x24Gb/s Crossbar, Interconnecting 128 Tiles in a Single Hop, and Occupying 6% of their Area”,

ACM/IEEE Symp. Networks-onChip (NOCS 2010), Grenoble, 2010, 9 pg.

G. Passas, M. Katevenis: “Asynchronous Operation of Bufferless Crossbars”, IEEE Conf. High Performance Switching Routing (HPSR 2007), Brooklyn, 2007, 6 pg.

G. Passas, M. Katevenis: “Packet-Mode Scheduling in Buffered Crossbar (CICQ) Switches”, IEEE Conf. High Performance Switching Routing (HPSR 2006), Poznan, 2006, 8 pg.

M. Katevenis, G. Passas: “Variable-Size Multipacket Segments in Buffered Crossbar (CICQ) Architectures”, IEEE Conf. Comm. (ICC 2005), Seoul, 2005, 6 pg.

M. Katevenis, G. Passas, D. Simos, I. Papaefstathiou, N. Chrysos: “Variable Packet Size Buffered Crossbar (CICQ) Switches”, IEEE Conf. Comm. (ICC 2004), Paris, 2004, 7 pg.

Technical Reports

G. Passas: “VLSI Micro-Architectures for High-Radix Crossbars”, FORTH-ICS/TR-427, 2012, 127 pg.

G. Passas: “VLSI Micro-Architectures for High-Radix Crossbars”, PhD Thesis, Univ. Crete, 2012, 136 pg.

G. Passas: “Packet-Mode Scheduling in Buffered Crossbar (CICQ) Switches”, MS Thesis, Univ. Crete, 2006, 83 pg.

G. Passas: “Performance Evaluation of Variable Packet Size Buffered Crossbar (CICQ) Switches”, FORTH-ICS/TR-328, 2003, 55 pg.

ACADEMIC RECORD

Talks

PhD Defense 2011, NOCS 2011, NOCS 2010, HiPEAC Comp. Sys. Week Barcelona 2010, HPSR 2007, HPSR 2006, ICC 2005

Teaching and 8-Year Teaching Assistant Experience

Grad course “CS-590.22: CMOS Technology for Computer Architects”, by FORTH-ICS and Univ. Crete for EuReCCA (S’12, w. Mavroidis & Katevenis)

Ugrad course “CS-120: Digital Design”, University of Crete (Fall’04, F’05, F’06, F’08, F’09)

Ugrad course “CS-225: Computer Organization”, University of Crete (Spring’04, S’05, S’06)

Grad course “CS-534: Packet Switch Architecture”, University of Crete (S’07, S’08, S’09, S’11)

8-Year Reviewer Experience

2013: IEEE Tran. VLSI, ACM Conf. Supercomp., ACM Tran. Embedded Comp. Sys.

2012: IEEE Tran. Parallel & Distr. Sys., IET Comp. & Digital Techniques.

2011: IEEE/ACM Symp. Microarch., IEEE Tran. VLSI, IEEE Tran. Computers.

2010: ACM/IEEE Symp. Networks on Chip.

2009: Elsevier Journal Parallel & Distr. Comp.

2007: IEEE Parallel & Distr. Processing Symp.

2006: ACM Conf. Supercomp., ACM/IEEE Symp. Arch. for Net. & Com. Sys., Euro-Par series Parallel & Distr. Comp., IEEE Conf. Comm.

2005: IEEE Global Telecomm. Conf

Academic Visit

Univ. Politecnica de Valencia, Dpto. Inf. de Sis. y Computadores (hosted by J. Duato, 2007)

Summer Schools

ACACES’2007: “Third Int’l Summer School on Advanced Computer Architecture and Compilation for Embedded Systems”, 2007, L’Aquila, Italy.

ACACES’2005: “First Int’l Summer School on Advanced Computer Architecture and Compilation for Embedded Systems”, 2005, L’Aquila, Italy.